departing from the scope of the example embodiments as defined by the appended claims.

1. (canceled)

2. A semiconductor device, comprising:

a light emitting structure including first and second conductivity-type semiconductor layers including $Al_xIn_yGa_{1-x-y})N$, wherein $0 \leq x < 1$, $0 \leq y < 1$, and $0 \leq x+y < 1$, and an active layer between the first and second conductivity-type semiconductor layers; and

an interconnection bump including:

an under bump metallurgy (UBM) layer on an electrode of at least one of the first and second conductivity-type semiconductor layers, the UBM layer having a first surface opposite to a surface of the electrode and a second surface extending from an edge of the first surface and connecting to the electrode;

an intermetallic compound (IMC) on the first surface of the UBM layer;

a solder bump bonded to the UBM layer with the IMC therebetween; and

a barrier layer on the second surface of the UBM layer and substantially preventing the solder bump from diffusing into the second surface of the UBM layer,

wherein the barrier layer includes an oxide layer containing at least one element of the UBM layer.

3. The semiconductor device of claim **2**, wherein a formation of the IMC or the solder bump is absent from the barrier layer.

4. The semiconductor device of claim **2**, wherein the barrier layer includes an oxide layer including at least one of nickel (Ni) and copper (Cu).

5. The semiconductor device of claim **2**, wherein the barrier layer has a lower level of wettability with respect to the IMC and the solder bump than a level of wettability with respect to the UBM layer.

6. The semiconductor device of claim **2**, wherein the second surface of the UBM layer has a structure slightly inclined towards the electrode from the first surface of the UBM layer.

7. The semiconductor device of claim **2**, wherein the second surface of the UBM layer is substantially perpendicular to the surface of the electrode.

8. The semiconductor device of claim **2**, wherein the UBM layer has a multilayer structure including a titanium (Ti) layer in contact with the electrode, and a Ni layer or a Cu layer on the Ti layer.

9. The semiconductor device of claim **2**, wherein the UBM layer has a multilayer structure including a chromium (Cr) layer in contact with the electrode, and a Ni layer or a Cu layer on the Cr layer.

10. The semiconductor device of claim **2**, wherein the UBM layer has a monolayer structure including one of a Ni layer or a Cu layer.

11. The semiconductor device of claim **2**, further comprising a passivation layer adjacent to the UBM layer on the electrode.

12. The semiconductor device of claim **11**, wherein the passivation layer is spaced apart from the UBM layer on the electrode.

13. The semiconductor device of claim **11**, wherein the passivation layer has a lower thickness than a thickness of the UBM layer.

14. A semiconductor device package comprising:

a mounting substrate;

a semiconductor device on the mounting substrate; and

an encapsulating portion encapsulating the semiconductor device,

wherein the semiconductor device includes:

a light emitting structure having a plurality of electrodes; and

an interconnection bump on the plurality of electrodes,

wherein the interconnection bump includes:

an under bump metallurgy (UBM) layer on the electrode, he UBM layer having a first surface opposite to a surface of the electrode and a second surface extending from an edge of the first surface and connecting to the electrode;

an intermetallic compound (IMC) on the first surface of the UBM layer;

a solder bump bonded to the UBM layer with the IMC therebetween; and

a barrier layer on the second surface of the UBM layer, the barrier layer substantially preventing the solder bump from diffusing into the second surface of the UBM layer.

15. The package of claim **14**, wherein the barrier layer includes an oxide layer containing at least one element of the UBM layer.

16. The package of claim **14**, wherein the encapsulating portion includes at least one type of phosphor.

17. A connection bump of a semiconductor device, the connection bump comprising:

at least one under bump metallurgy (UBM) layer on an electrode of the semiconductor device;

an intermetallic compound (IMC) on the UBM layer;

a solder bump on the IMC; and

a barrier layer between the UBM layer and the IMC, the barrier layer being configured to substantially prevent at least one of the solder bump and the IMC from diffusing into the UBM layer.

18. The connection bump of claim **17**, wherein the barrier layer extends on a surface of the UBM layer that extends between the IMC and the electrode.

19. The connection bump of claim **17**, wherein the barrier layer has a level of wettability with respect to at least one of the IMC and the solder bump such that at least one of the IMC and the solder bump cannot be formed on the barrier layer.

20. The connection bump of claim **17**, wherein the barrier layer includes an oxide layer having at least one element of the UBM layer.

21. The connection bump of claim **17**, wherein the UBM layer comprises at least a first layer and a second layer, the first layer being in contact with the electrode,

wherein the first layer includes at least titanium, and the second layer includes at least one of nickel and copper.

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